CLAIMS

What is claimed is:

1. A delay lock loop (DLL) circuit coupled between output and input terminals of a clock network, the DLL circuit comprising:

an input clock terminal;

a feedback clock terminal coupled to the output terminal of the clock network;

a delay line having an input terminal coupled to the input clock terminal and having a plurality of output terminals providing a plurality of intermediate clock signals;

a control circuit having a first input terminal coupled to the feedback clock terminal, a second input terminal coupled to the input clock terminal, and a plurality of control output terminals; and

a bi-directional shift register and clock multiplexer having a plurality of data input terminals coupled to the output terminals of the delay line, a plurality of control input terminals coupled to the control output terminals of the control circuit, and an output terminal coupled to the input terminal of the clock network,

wherein the bi-directional shift register comprises a token bit shifted under control of the control circuit, and

wherein the clock multiplexer selects one of the intermediate clock signals, as determined by a location of the token bit within the bi-directional shift register, to supply to the output terminal.

2. The DLL circuit of Claim 1, wherein the output terminal of the bi-directional shift register and clock multiplexer is coupled to a third input terminal of the control circuit.

3.   The DLL circuit of Claim 1, wherein:
     the control circuit comprises a shift clock generator
circuit and a shift enable circuit;
     the shift clock generator circuit provides a plurality
of control signals to a first subset of the control input
terminals of the bi-directional shift register and clock
multiplexer; and
     the shift enable circuit provides a plurality of shift
enable signals to a second subset of the control input
terminals of the bi-directional shift register and clock
multiplexer.

4.   The DLL circuit of Claim 3, wherein:
     the output terminal of the bi-directional shift register
and clock multiplexer is coupled to a third input terminal of
the control circuit; and
     the shift clock generator circuit comprises a clock
divider circuit having an input terminal coupled to the third
input terminal of the control circuit.

5.   The DLL circuit of Claim 4, wherein the clock divider
circuit is programmable.

6.   The DLL circuit of Claim 1, wherein the bi-directional
shift register and clock multiplexer comprises a plurality of
shift register circuits coupled together through a plurality
of multiplexer circuits, each of the shift register circuits
being bi-directional and storing an associated token bit,
each succeeding one of the shift register circuits comprising
a smaller number of memory elements and each succeeding one
of the multiplexer circuits comprising a smaller number of
multiplexers until a single one of the shifted intermediate
clocks signals has been selected.

7.   The DLL circuit of Claim 6, wherein each succeeding one
of the shift register circuits comprises exactly half as many

memory elements as a preceding shift register circuit, and each succeeding one of the multiplexer circuits comprises exactly half as many multiplexers as a preceding multiplexer circuit.

8. A system, comprising:

a clock network having an input terminal and an output terminal; and

a delay lock loop (DLL) circuit coupled between the output and input terminals of the clock network, the DLL circuit comprising:

an input clock terminal;

a feedback clock terminal coupled to the output terminal of the clock network;

a delay line having an input terminal coupled to the input clock terminal and having a plurality of output terminals providing a plurality of intermediate clock signals;

a control circuit having a first input terminal coupled to the feedback clock terminal, a second input terminal coupled to the input clock terminal, and a plurality of control output terminals; and

a bi-directional shift register and clock multiplexer having a plurality of data input terminals coupled to the output terminals of the delay line, a plurality of control input terminals coupled to the control output terminals of the control circuit, and an output terminal coupled to the input terminal of the clock network,

wherein the bi-directional shift register comprises a token bit shifted under control of the control circuit, and

wherein the clock multiplexer selects one of the intermediate clock signals, as determined by a location of the token bit within the bi-directional shift register, to supply to the output terminal.

9.   The system of Claim 8, wherein the output terminal of the
bi-directional shift register and clock multiplexer is
coupled to a third input terminal of the control circuit.

10.   The system of Claim 8, wherein:
     the control circuit comprises a shift clock generator
circuit and a shift enable circuit;
     the shift clock generator circuit provides a plurality
of control signals to a first subset of the control input
terminals of the bi-directional shift register and clock
multiplexer; and
     the shift enable circuit provides a plurality of shift
enable signals to a second subset of the control input
terminals of the bi-directional shift register and clock
multiplexer.

11.   The system of Claim 10, wherein:
     the output terminal of the bi-directional shift register
and clock multiplexer is coupled to a third input terminal of
the control circuit; and
     the shift clock generator circuit comprises a clock
divider circuit having an input terminal coupled to the third
input terminal of the control circuit.

12.   The system of Claim 11, wherein the clock divider
circuit is programmable.

13.   The system of Claim 8, wherein the bi-directional shift
register and clock multiplexer comprises a plurality of shift
register circuits coupled together through a plurality of
multiplexer circuits, each of the shift register circuits
being bi-directional and storing an associated token bit,
each succeeding one of the shift register circuits comprising
a smaller number of memory elements and each succeeding one
of the multiplexer circuits comprising a smaller number of

multiplexers until a single one of the shifted intermediate
clocks signals has been selected.

14. The system of Claim 13, wherein each succeeding one of
the shift register circuits comprises exactly half as many
memory elements as a preceding shift register circuit, and
each succeeding one of the multiplexer circuits comprises
exactly half as many multiplexers as a preceding multiplexer
circuit.

15. A method of synchronizing a feedback clock signal from a
clock network with an input clock signal, the method
comprising:
        receiving the feedback clock signal;
        receiving the input clock signal;
        providing from the input clock signal a plurality of
intermediate clock signals delayed from the input clock
signal by incremental unit delays;
        shifting a first token bit in either of two directions
within a first shift register;
        selecting from among the intermediate clock signals a
selected clock signal based on a location of the first token
bit within the first shift register; and
        providing the selected clock signal to the clock
network.

16. The method of Claim 15, further comprising:
        shifting a second token bit in either of the two
directions within a second shift register,
        wherein selecting from among the intermediate clock
signals the selected clock signal based on the location of
the first token bit within the first shift register further
comprises selecting from among the intermediate clock signals
the selected clock signal based on a location of the second
token bit within the second shift register.

17. The method of Claim 16, wherein the second shift register comprises exactly half as many memory elements as the first shift register.

18. The method of Claim 15, further comprising:
verifying, prior to shifting the first token bit in either of two directions, that a selected one of the two directions is compatible with a position of the first token bit within the first shift register.

19. A system for synchronizing a feedback clock signal from a clock network with an input clock signal, the system comprising:
means for receiving the feedback clock signal;
means for receiving the input clock signal;
means for providing from the input clock signal a plurality of intermediate clock signals delayed from the input clock signal by incremental unit delays;
means for shifting a first token bit in either of two directions within a first shift register;
means for selecting from among the intermediate clock signals a selected clock signal based on a location of the first token bit within the first shift register; and
means for providing the selected clock signal to the clock network.

20. The system of Claim 19, further comprising:
means for verifying that a selected one of the two directions is compatible with a position of the first token bit within the first shift register.

21. A multiplexer circuit, comprising:

N data input terminals, wherein N is an integer;

an output terminal;

a first bi-directional shift register comprising N bits and N output terminals, wherein exactly one of the N bits has a first token value;

an N-to-M multiplexer comprising N data input terminals coupled to the N data input terminals of the multiplexer circuit, N control terminals coupled to the N output terminals of the first bi-directional shift register, and M output terminals, wherein M is an integer less than N;

a second bi-directional shift register comprising M bits and M output terminals, wherein exactly one of the M bits has a second token value; and

an M-to-1 multiplexer comprising M data input terminals coupled to the M data output terminals of the N-to-M multiplexer, M control terminals coupled to the M output terminals of the second bi-directional shift register, and an output terminal coupled to the output terminal of the multiplexer circuit.

22. The multiplexer circuit of Claim 21, wherein N is two times M.

23. The multiplexer circuit of Claim 21, wherein the first and second token values are high values.

24. The multiplexer circuit of Claim 21, wherein the first and second token values are the same value.